

25.1 A Multipath Technique for Canceling Harmonics and Sidebands in a Wideband Power Upconverter

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Amplifiers and mixers not only produce a useful amplified or frequency-shifted signal, but also many unwanted harmonics and sidebands caused by nonlinearity and time-variance. Filters are commonly used to clean up the spectrum, but are application specific and often difficult to integrate. Zero-order-hold filtering in a mixer-DAC [2] reduces DAC-related spurs, but does not remove harmonics generated in the mixer. A harmonic-rejection mixer canceling the third- and fifth-order harmonics [3] does relax analog filter requirements. In this paper, we exploit the practical potential of the polyphase multipath circuit theory proposed in [1] to further reduce or even completely eliminate filters by canceling a very large multitude of harmonics and sidebands. As a demonstration, we apply the technique to realize a wideband *filter-less* power upconverter for possible future multi-standard radio applications in CMOS.

Figure 25.1.1 shows a polyphase n -path circuit consisting of n identical memory-less weakly nonlinear circuits [1]. The basic idea is to apply a phase shift $(i-1)\times 2\pi/n$ before and after the nonlinear circuit in each path i , with equal but opposite phase. An input sine wave results in 1^{st} -order harmonic components produced by the n paths, which are in phase and add constructively. However, nonlinearities produce higher harmonics with a phase proportional to the order of the harmonic, and the contributions of different paths can cancel each other except for the $(j\times n+1)^{\text{th}}$ harmonic, where j is an integer [1]. Similar conclusions hold for inter-modulation products. In general, if the number of paths is higher, more harmonics and sideband products can be cancelled.

Figure 25.1.2 shows the power upconverter (PU) we implemented, which combines mixer and power amplifier functionality with 18 paths contributing current to the load. Since the desired output signals all add up in phase, the total area and power of the PU-core is not increased by dividing it into 18 sections. Each path consists of a switched transistor mixer [4] wherein a baseband (BB) signal is applied to a differential pair acting as transistor that is activated by a local oscillator signal (LO) driving a grounded switch. The operation of this circuit essentially adds the phase of the LO to the phase of the BB signal. The different LO phases are generated on chip while the 18 BB signals (9 differential) are generated off chip, but should ultimately be generated by a BB processor using DACs. Using a square-wave LO signal and large output swing is good for the efficiency, but also produces many harmonics and sidebands at frequencies $k\omega_{LO} \pm m\omega_{bb}$, where k and m are integers. The products that are cancelled by the multipath technique are indicated by M in the table in Fig. 25.1.3 for an 18-path system. However, products like $2\omega_{LO} + 2\omega_{bb}$, $3\omega_{LO} + 3\omega_{bb}$, or $4\omega_{LO} + 4\omega_{bb}$ have a phase of 0° at the output of each path and cannot be cancelled by the multipath technique [1]. Among these non-cancelled harmonics, the ones like $2\omega_{LO} + 2\omega_{bb}$, or $4\omega_{LO} + 4\omega_{bb}$ are cancelled by the use of a differential transistor ("B" in Fig. 25.1.3). To eliminate the strong $3\omega_{LO} + 3\omega_{bb}$ harmonic, we use a LO with 1/3 duty cycle, so that the 3^{rd} -harmonic term disappears from the Fourier series expansion ("D" in Fig. 25.1.3). Other non-cancelled products like $5\omega_{LO} + 5\omega_{bb}$ and $7\omega_{LO} + 7\omega_{bb}$ are typically smaller than residual products caused by inaccuracies like device and phase mismatch [1].

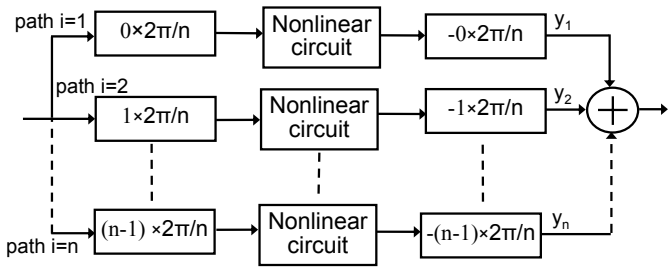
To maximize the experimental flexibility and frequency range, we implemented the clock-generation "brute-force" via a shift-register running at 9 times the LO frequency to generate 18 different phases. The 1/3 duty-cycle is implemented via the NOR-feedback loop in Fig. 25.1.2.

The proposed PU is fabricated in a 0.13 μm CMOS process with a supply voltage of 1.2V and has an option to select 6 or 18 paths. The die micrograph is shown in Fig. 25.1.7 and the chip has an active area of 0.14mm². The RF chokes (RFC) and load are off-chip. No filters are used. Operating each individual mixer at the 1dB-compression point, the PU is designed for large output swing (2.54V_{pp, diff}) at the output to get good efficiency. It delivers 8mW output power to a 100 Ω load with a drain efficiency of 11%. The BB bandwidth is 0 to 50MHz, but the input signal was arbitrarily chosen at 100kHz, while varying the LO frequency between 0 and 2.4GHz. Figure 25.1.4 shows the output frequency spectrum (350MHz carrier) before and after the cancellation for a single path (upper) and multipath circuit (lower figure). Please note that the unfortunate FM radio spurs that are modulated with our output signal are caused by a 100.0MHz FM radio broadcast transmitter on the roof of our building. The suppression of the products having 3rd, 6th, 9th harmonics of the LO in the top plot in Fig. 25.1.4 is caused by the 1/3 duty-cycle of the LO signal. All the harmonic products are effectively suppressed to -48dBc. The top plot in Fig. 25.1.5 shows -39dBc of sideband suppression as well as LO leakage and image rejection. The lower plot in Fig. 25.1.5 shows the first non-cancelled harmonic $17\omega_{LO} + \omega_{bb}$ at 1.3601GHz for a "low frequency" 80MHz carrier. The output spectrum is clean with -46dBc of rejection up to the 17th harmonic of the LO. Figure 25.1.6 shows the wideband property of the PU. The 6- and 18-path PUs work for output frequencies up to 2.4GHz and 800MHz (at 7.2GHz clock) respectively. The total power consumption of the chip is 228mW; 156mW by the digital circuits (dividers and buffers) and 72mW by the PU core. The high power consumption of the digital circuit is due to the brute-force multiple phase generation via 9x-higher frequency, and the use of high bias currents in the current-mode logic. The digital power can be significantly reduced in a real application by using, for instance, a DLL running at the LO frequency. The magnitudes of the cancelled harmonics depend on matching, both in time and magnitude. Identical paths and loads are used to reduce the phase mismatches between paths. We also measured multiple samples of the IC, and all 20 samples showed very similar behavior within 1 to 2dB.

In summary, a multipath approach in combination with a LO with 1/3 duty-cycle results in a power upconverter with a clean output spectrum. It operates from dc to 2.4GHz with worst-case harmonic rejection of -40dBc. It uses no filters, but only digital blocks and switched transistor mixers, enabling this design to fit in future software defined radio architectures. The frequency range limitation in the clock generator will be relaxed in newer CMOS technologies.

References:

- [1] E. Mensink, E.A.M. Klumperink, B. Nauta, "Distortion Cancellation by Polyphase Multipath Circuits," *IEEE T. Circuits and Systems I*, pp. 1785-1794, Sept., 2005.
- [2] J. A. Weldon et al., "A 1.75-GHz Highly Integrated Narrow-Band CMOS Transmitter with Harmonic-Rejection Mixers," *IEEE J. Solid-State Circuits*, vol. 36, pp. 2003-2015, Dec., 2001.
- [3] P. Eloranta et al., "Direct-Digital RF Modulator IC in 0.13 μm CMOS for Wide-Band Multi-Radio Applications," *ISSCC Dig. Tech. Papers*, pp. 532-533, Feb., 2005.
- [4] E.A.M. Klumperink et al., "A CMOS Switched Transistor Mixer," *IEEE J. Solid-State Circuits*, Vol. 39, No. 8, pp. 1231-1240, Aug., 2004.



3-Phase Example:

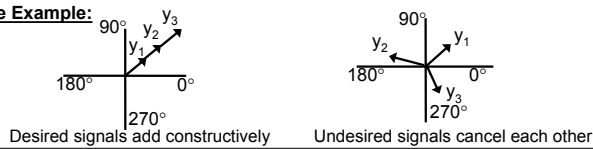


Figure 25.1.1: n-path polyphase circuit and phasor diagram for a 3-path circuit showing the 1st harmonic (left) and 3rd harmonic (right).

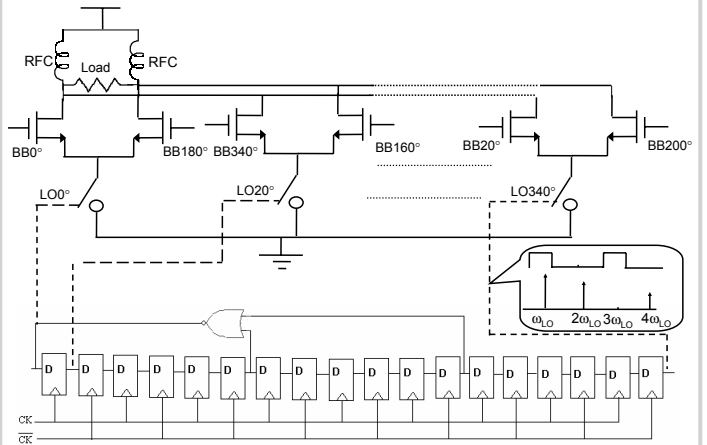


Figure 25.1.2: Power upconverter using a polyphase 18-path architecture.

m →	-4	-3	-2	-1	0	1	2	3	4
1ω _{LO} +mω _{BB}	BM	M	BM	M	M		BM	M	BM
2ω _{LO} +mω _{BB}	BM	M	BM	M	M	M	B	M	BM
3ω _{LO} +mω _{BB}	BMD	MD	BMD	MD	M	MD	BMD	D	BMD
4ω _{LO} +mω _{BB}	BM	M	B	M	M	M	BM	M	B
5ω _{LO} +mω _{BB}	BM	M	BM	M	M	M	BM	M	BM
6ω _{LO} +mω _{BB}	BMD	MD	BMD	MD	M	MD	BMD	MD	BMD
7ω _{LO} +mω _{BB}	BM	M	BM	M	M	M	BM	M	BM
8ω _{LO} +mω _{BB}	BM	M	BM	M	M	M	BM	M	BM
9ω _{LO} +mω _{BB}	BMD	MD	BMD	MD	M	MD	BMD	MD	BMD
10ω _{LO} +mω _{BB}	BM	M	BM	M	M	M	BM	M	BM
11ω _{LO} +mω _{BB}	BM	M	BM	M	M	M	BM	M	BM
12ω _{LO} +mω _{BB}	BMD	MD	BMD	MD	M	MD	BMD	MD	BMD
13ω _{LO} +mω _{BB}	BM	M	BM	M	M	M	BM	M	BM
14ω _{LO} +mω _{BB}	B	M	BM	M	M	M	BM	M	BM
15ω _{LO} +mω _{BB}	BMD	D	BMD	MD	M	MD	BMD	MD	BMD
16ω _{LO} +mω _{BB}	BM	M	B	M	M	M	BM	M	BM
17ω _{LO} +mω _{BB}	BM	M	BM		M	M	BM	M	BM

M=canceled by multi-path, D=canceled by 33% duty cycle, B=canceled by balancing

Figure 25.1.3: Table showing the cancellation of unwanted products with different techniques.

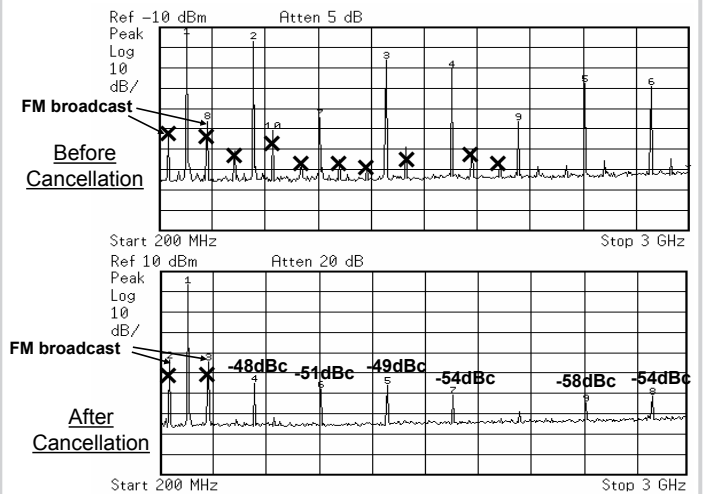


Figure 25.1.4: Output spectrum before and after cancellation ('X' see text).

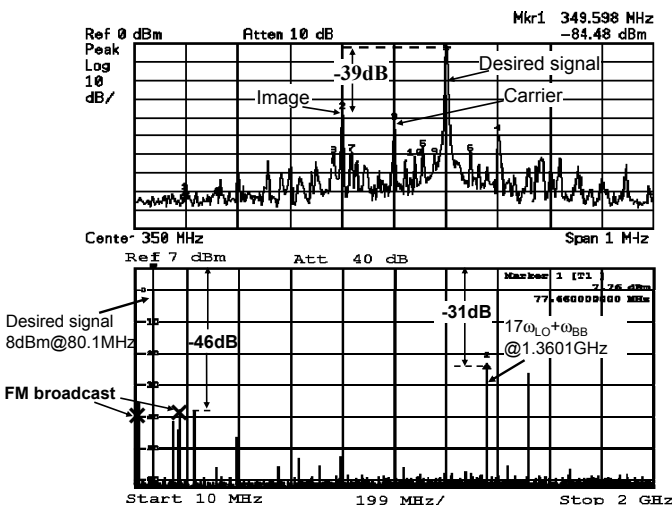


Figure 25.1.5: LO leakage and image rejection performance (upper), and output spectrum for 80MHz carrier (lower).

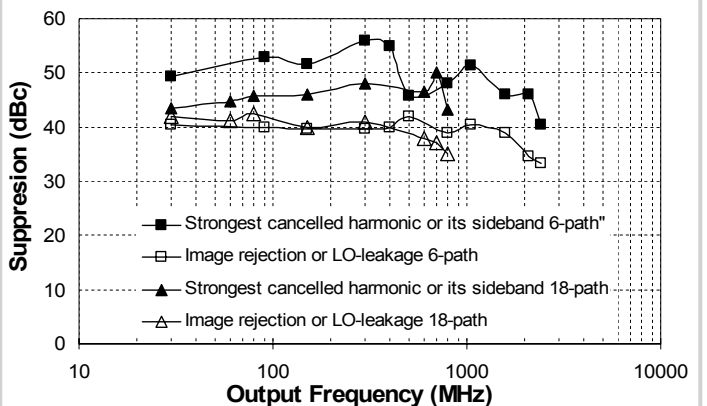


Figure 25.1.6: Measured suppression of undesired products over the full output frequency range.

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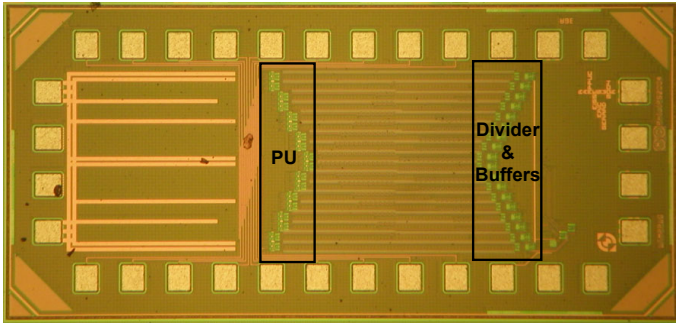


Figure 25.1.7: Chip micrograph.